2185#6
BT

Patent

Docket No.: CYPR-CD00174

3-5-03

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.					
Date of Deposit:	02/19/03	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Monte Mar and Warren Snyder

Serial No.: 09/930,021 Group Art Unit:

Filed: 08/14/01 Examiner:

Title: PROGRAMMING METHODOLOGY AND ARCHITECURE FOR A PROGRAMMABLE ANALOG SYSTEM (AS AMENDED)

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
..X.. Information Disclosure statement (2 sheets)
..... Information Disclosure statement and late filing fee
..X.. Form 1449
..... Petition for Extension of Time
..X.. Other: REFERENCES
..X.. Other: Related US Pending Patent applications

Fee Calculation (for other than a small entity)

Fee Items	Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere	$ .00	$0.00
Information Disclosure Statement, late filing	$180.00	$0.00
Other:		$0.00
Total Fees		$0.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

kgr 7/98

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 2/19/07

By: _____
Anthony C. Murabito
Reg. No. 35,295

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: CYPR-CD00174

Inventor(s): Monte Mar and Warren Snyder

Serial No.: 09/930,021 Group Art Unit:

Filed: 08/14/01 Examiner:

Title: PROGRAMMING METHODOLOGY AND ARCHITECURE FOR A PROGRAMMABLE ANALOG SYSTEM (AS AMENDED)

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
6,144,327	PROGRAMMABLY INTERCONNECTED PROGRAMMABLE DEVICES	11/07/00
5,202,687	ANALOG TO DIGITAL CONVERTER	04/13/93
6,166,367	PROGRAMMABLE ANALOG ARITHMETIC CIRCUIT FOR IMAGING SENSOR	12/26/00
5,600,262	INTEGRATED CIRCUIT FACILITATING SIMULTANEOUS PROGRAMMING OF MULTIPLE ANTIFUSES	02/04/97
5,414,308	HIGH FREQUENCY CLOCK GENERATOR WITH MULTIPLEXER	05/09/95
5,258,760	DIGITALLY DUAL-PROGRAMMABLE NTEGRATOR CIRCUIT	11/02/93
5,563,526	PROGRAMMABLE MIXED-MODE INTEGRATED CIRCUIT ARCHITECTURE	10/08/96
6,225,866	SERIES CONNECTED MULTISTAGE LINEAR FET AMPLIFIER CIRCUIT	05/01/01

The Examiner's attention is respectfully directed to the following related pending U.S. Patent Applications:

CYPR-CD00173; " A PROGRAMMABLE ANALOG SYSTEM ARCHITECTURE (AS AMENDED)"; 07/18/01; 09/909,047; Mar

CYPR-CD00175; "METHOD FOR SYNCHRONIZING AND RESETTING CLOCK SIGNALS SUPPLIED TO MULTIPLE PROGRAMMABLE ANALOG BLOCKS (AS AMENDED)"; 10/01/01; 09/969,311; B. Sullam

CYPR-CD00194; "METHOD AND APPARATUS FOR LOCAL AND GLOBAL POWER MANAGEMENT IN A PROGRAMMABLE ANALOG CIRCUIT"; 08/22/01; 09/935,454; M. Mar

CYPR-CD00232; "PROGRAMMABLE SYSTEM ON A CHIP"; 10/01/01; 10/033,027; W. Snyder

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 2/19/07

By: _____
Anthony C. Murabito
Reg. No. 35,295